Amendments to the Claims

1. (*Currently Amended*) Method for manufacturing an array of semiconductor devices on a substrate ~~(10)~~, each device having a floating gate ~~(36)~~, comprising:

[[-]] first forming isolation zones ~~(14)~~ in the substrate ~~(10)~~,

[[-]] thereafter forming a floating gate separator ~~(32)~~ on the isolation zones ~~(14)~~ at locations where separations between adjacent floating gates ~~(36)~~ are to be formed,

[[-]] after forming the floating gate separator ~~(32)~~, forming the floating gates ~~(36)~~ on the substrate ~~(10)~~ between parts of the floating gate separator ~~(32)~~, and

[[-]] thereafter removing the floating gate separator ~~(32)~~ so as to obtain slits in between neighboring floating gates ~~(36)~~.

2. (*Currently Amended*) Method according to claim 1, furthermore comprising, after forming of the floating gate separator ~~(32)~~ and before forming of the floating gate ~~(36)~~, reducing the dimensions of the floating gate separator ~~(32)~~.

3. (*Currently Amended*) Method according to claim 2, wherein the dimensions of the floating gate separator ~~(32)~~ are reduced to sub-lithographic dimensions.

4. (*Currently Amended*) Method according to claim 3, wherein the dimensions of the floating gate separator ~~(32)~~ are reduced to between 100 nm and 40 nm.

5. (*Currently Amended*) Method ~~according to any of claims 2 to 4,~~ according to claim 2, wherein the dimensions of the floating gate separator ~~(32)~~ are reduced by resist shrink.

6. (*Currently Amended*) Method ~~according to any of claims 2 to 5,~~ according to claim 2, wherein the dimensions of the floating gate separator ~~(32)~~ are reduced by trim plasma etching.

7. (*Currently Amended*) Method ~~according to any of claims 2 to 6,~~ according to claim 2, wherein the dimensions of the floating gate separator ~~(32)~~ are reduced by an isotropic over-etch of the floating gate separator ~~(32)~~.

8. (*Currently Amended*) Method ~~according to any of claims 2 to 7,~~ according to claim 2, wherein the dimensions of the floating gate separator ~~(32)~~ are reduced by phase-shift lithography.

9. (*Currently Amended*) Method ~~according to any of the previous claims,~~ according to claim 2, wherein the floating gate separator ~~(32)~~ comprises nitride material.

10. (*Currently Amended*) Method ~~according to any of the previous claims,~~ according to claim 2, wherein the floating gate separator ~~(32)~~ comprises at least two layers of different material.

11. (*Currently Amended*) Method ~~according to any of the previous claims,~~ according to claim 2, furthermore comprising forming spacers ~~(44)~~ next to the floating gate separator ~~(32)~~ before forming the floating gates ~~(36)~~.

12. (*Currently Amended*) An array of semiconductor devices with a floating-gate to control-gate coupling ratio, comprising:

[[-]] a substrate ~~(10)~~ with a planar surface ~~(12)~~,

[[-]] an isolation zone ~~(14)~~ in the substrate ~~(10)~~ in the planar surface ~~(12)~~,

[[-]] at least two floating gates ~~(36)~~ extending on the substrate ~~(10)~~ in a first direction, each floating gate ~~(36)~~ partially overlapping the isolation zone ~~(14)~~ and comprising floating gate material,

[[-]] a slit between the two floating gates ~~(36)~~, and

[[-]] a control gate ~~(40)~~ extending laterally with respect to the planar surface ~~(12)~~ over the floating gates ~~(36)~~,

[[-]] wherein at least one of the floating gates ~~(36)~~ is provided with a sharp tip ~~(46)~~ of floating gate material both in the first direction and in a second direction including an angle with the first direction.

13. (*Original*) Array of semiconductor devices according to claim 12, wherein the slit is a sub-lithographically dimensioned slit.

14. (*Currently Amended*) Array of semiconductor devices ~~according to any of claims 12 or 13,~~ according to claim 12, wherein at least one of the floating gates ~~(36)~~ has a flat top surface.

15. (*New*) Array of semiconductor devices according to claim 13, wherein at least one of the floating gates has a flat top surface.